

size of solid electrolyte elements(110)is in the range of about 1-50nm (electrolyte in the range of 25-75 nm, see column 3, paragraph 0037).

The applicant disagrees above explanation about Figure 3 of Gilton's invention (US.2003/0194865). The memory cell is a basic unit in memory and one cell represents a data "bit". The main difference between the memory cell of the applicant and conventional programmable metallization cell (PMC) is that the memory cell in applicant's invention consists of a plurality of resistive elements, while the memory cell in conventional PMC cell, such as disclosed in the publication (US.2003/0194865) consists if one resistive element. This difference comes from the different process used in the memories. In conventional PMC memory, the photolithography normally is used to define the resistive element size which is limited by the resolution of the photolithography. To minimize the sizes for both memory cell and resistive element size, memory cell normally consists of one element. While in applicant's invention, a co-deposition of thin film is used. A memory cell normally consists of a plurality of resistive elements which are in nano-scale in diameter and randomly distributed. Therefore, the key differences of applicant's invention from the conventional PMC memory cell are the multiple resistive elements in an individual cell and much smaller element size. Due to the much smaller resistive element, the total volume of resistive elements in an individual cell is also smaller and thus the power consumption is also lower.

In the publication (US.2003/0194865) Gilton shows in Figure 3 an exemplary memory cell with single resistive element. It is a conventional PMC memory cell structure. The resistive element comprises a layer of electrolyte 110 which is 25-75 nm thick over which is a layer of metal 112 (such as Ag) with thickness of 5-25 nm. The layers were patterned to form a pillar-shaped resistive element. One memory cell consists of only one resistive element.

In the applicant's invention, the memory cell consists of a plurality of resistive elements with size of 1-50 nm. Comparing memory cell structure of applicant's invention (Figure 1 and 6) and that of Gilton (Figure 2), they are completely different in terms of structure and size.

Response to Arguments

Applicant argue, on page 2, paragraph 1, that Gilton fail to discloses a resistive layer with "a plurality of solid electrolyte" embedded therewithin and metal layer there on.

Examiner disagrees, Gilton disclosed a metal film (112) is deposited over a resistive layer (110) formed of electrolyte element, see paragraph 0024.

Applicant has not claimed any special arrangement or types of electrolyte element.

Applicant has claimed a memory cell structure with a plurality of resistive elements with small size. A layer with a plurality of solid electrolyte elements embedded in an insulator and a thinner layer of metal constitute resistive element as claimed in claims 32 and 33.

Applicant argues, on page 2, paragraph 2, the memory cell of Gilton includes only pillar. The pillar structure of Gilton is completely different from the cell structure of applicant.

Examiner disagrees. Applicant has not claimed any specific configuration to differentiate the claimed structure from that shown by Gilton.

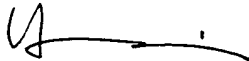
Applicant has claimed a memory cell structure with a plurality of resistive elements with small size. A layer with a plurality of solid electrolyte elements embedded in an insulator and a thinner layer of metal constitute resistive element as claimed in claims 32 and 33. Gilton's memory is a conventional PMC memory cell structure. The resistive element comprises a layer of electrolyte 110 which is 25-75 nm thick over which is a layer of metal 112 (such as Ag) with thickness of 5-25 nm. They are obviously different in terms of structure and size.

Based on the above reasons, applicant requests the examiner to withdraw the rejection.

Conditional Request for Constructive Assistance

Applicant has amended the specification and claims of this application so that they are proper, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, applicant respectfully request the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P. § 2173.02 and § 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

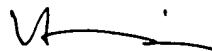
Very respectfully,



Hai Jiang

Certificate of Mailing: I certify that on the date below this document and referenced attachments, if any, will be deposited with the USPS as express mail (Label #: ED 812040216 US) with proper postage affixed in an envelope addressed to "Commissioner for Patents, Alexandria, Virginia 22313-1450"

Aug. 18, 2006

 (Hai Jiang)